IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
PATENT APPLICATION

Appl. No.	:	10/631,083	Confirmation No. 2030
Applicant	:	Morio Nakao	
Filed	:	July 31, 2003	
TC/A.U.	:	2822	
Examiner	:	Graybill, David E	
Docket No.	:	TI-35373	
Customer No.	:	23494	

BRIEF ON APPEAL

M. S. Appeal Brief-Patents
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In support of his appeal of the Final Rejection of claims in this application, applicant respectfully submits this brief.

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated, a Delaware corporation with offices at 7839 Churchill Way, Dallas, Texas 75251.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals or interferences.

STATUS OF CLAIMS

This is an appeal of claims 18, and 19. Claims 1 through 9, 11, and 13 have been canceled from this examination; and claims 10, 12, 14 through 17 stand rejected but are not under this appeal.

STATUS OF AMENDMENTS

Appellant filed an amendment in response to the final rejection of August 14, 2006. The amendment was denied entry.

SUMMARY OF CLAIMED SUBJECT MATTER

Claim 18 is an independent claims and claim 19 depends from claim 18.

Claim 18 describes a method for packaging an integrated circuit chip. It includes the following steps:

a. providing an integrated circuit chip;[1]

b. providing an insulating carrier tape[2] with a patterned metal layer[3] with a first side adhering to the insulating carrier tape;[4]

c. positioning the integrated circuit chip over a second side of the metal layer and electrically connecting the integrated circuit chip to the metal pattern;[5]

d. encapsulating the chip and the electrical connections;[6]

e. removing the carrier tape to uncover the entire first side of the metal layer;[7] and

f. then applying an insulating layer[8] to the first side uncovering a portion of the first side of the patterned metal layer.[9]

Claim 18 depends from claim 17 with the additional limitation that the insulating layer be thinner than the insulating carrier tape.[10]

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[1] This application, page 8, line 21, Fig. 2, element 206.
[2] Id. line 24 through 25, element 201.
[3] Id. line 7 through 8, element 202.
[4] Id. lines 13 through 16.
[5] Id. lines 18 through 24.
[6] Id. lines 24 through 26.
[7] Id. lines 27 through 32.
[8] Id. page 9, lines 8 through 12, element 401.
[9] Id. lines 8 through 17.
[10] Id. page 8, lines 8 through 10 and page 9, lines 8 through 9.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Both claims 18 and 19 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Fukutomi.[11]

ARGUMENTS

1. The Fukutomi et al. reference does not disclose the claim elements in claim 18 as asserted in the Office Action and therefore does not render claim 18, as a whole, obvious.

The Examiner rejected claim 18, together with claims 10, 14, and 19 in six pages of Office Action, based on 'paragraphs 6-8, 98, 128, 168, 170-173, as the "seventeenth embodiment, …"' [12] of the Fukutomi publication.

The Fukutomi publication demonstrates "the seventeenth embodiment" in two specific examples, following a general description of the embodiment:

> [0167] With reference to FIGS. 19, 20 and 21, a description will be given of the seventeenth embodiment of the present invention. [13]

First, Fukutomi introduces a set of wiring patterns and a supporting member, which the Office Action suggests discloses the carrier tape element in claim 18:

> [0168] Plural sets of predetermined wiring patterns 52 are formed on a supporting member 51 (FIG. 19a). As the supporting member, an insulating base material such as a polyimide film can be used besides a metal foil such as an electrolytic copper foil.[14]

Since element (b) of claim 18 requires an insulating carrier tape, supporting members made of metal foil would not anticipate the carrier tape of claim 18; and it is only necessary to follow the method in Fukutomi relating to the supporting member of "insulating base material" such as a polyimide film:

> When an insulating base material is used, there are two methods. According to the first method, nonthrough-holes reaching the wiring patterns are formed at predetermined positions of the insulating base material, and external connection terminals are formed at exposed portions of the wiring patterns. The nonthrough-holes can be formed by applying an excimer laser or a CO_2 laser and so on. According to the second method, a drilled insulating base material provided with an adhesive is formed in advance and,

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[11] U.S. Pat. Pub. No. 2002/0094606, pub. Jul. 18, 2002, from an application filed Jan. 8, 2002 by Naoki Fukutomi et al.
[12] The Office Action, Aug. 14, 2006, page 3.
[13] Fukutomi, supra, ¶ [0167].
[14] Id. ¶ [0168].

> subsequent to lamination with an electrolytic copper foil or the like, the copper foil is subjected to etching.[15]

The next paragraph of the Fukutomi publication describes the preparation of a metallic supporting member, which is not applicable to claim 18. In the following paragraph, Fukutomi picks up the process at the step of attaching the semiconductor device 54:

> [0170] Next, after semiconductor devices 54 are mounted by die-bonding materials 53, terminals of the semiconductor devices and wiring patterns are electrically connected (FIG. 19b), and plural sets of the semiconductor devices and wiring patterns are all together sealed with a resinous sealing material 56 by the transfer molding process (FIG. 19c).[16]

After the molding process, the Fukutomi method bifurcates. If the supporting member is metallic, Fukutomi discloses a process step of removing the metallic member; on the other hand, if the supporting member is insulating base material, as in claim 18, the Fukutomi publication specifically discloses that instead of "removing the carrier tape to uncover the entire first side of the metal layer" as required in claim 18, it is "only necessary to selectively remove the insulating base material at predetermined areas":

> Where the supporting member is a metal foil, the supporting member is removed by a chemical etching process and external connection terminals 57 are formed at predetermined positions (FIG. 19d). When an insulating base material is used as a supporting member, it is only necessary to selectively remove the insulating base material at predetermined areas by a laser or the like. Finally, the substrate which has been sealed as a whole is cut apart into unit portions 58. Incidentally, a solder resist layer may be formed on exposed surfaces of the wiring patterns for protecting the wiring patterns.[17]

To summarize the relevant portion of the Fukutomi publication, what is disclosed in the Fukutomi publication is a method of making a semiconductor package with either a metallic supporting member or an insulating supporting member. When the supporting member is metallic, it is necessary to remove it after the molding process less all the wiring patterns are electrically shorted. If the supporting member is insulating, however, it is only necessary to selectively remove the insulating base material at predetermined areas either after the package is molded, or before the metal patterns are affixed to the supporting member. The

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[15] Id. lines 5 through 11.
[16] Id. ¶ [170].
[17] Id. last eleven lines.

removal of the "selective" areas of the insulating support member is so that "external connection terminals are formed at exposed portions of the wiring patterns."[18]

Compared to claim 18, which requires removing the carrier tape to uncover the entire first side of the metal layer, the Fukutomi publication falls short.

The solder resist layer disclosed in the above cited paragraph applies to a metallic supporting member and does not apply to an insulating supporting member. According to the Fukutomi process, the only exposed areas of the wiring patterns as a result of the removal of an insulating supporting member by "a laser or the like" will be covered with "external connection terminals"; the rest of the metal pattern areas are covered and protected by the remaining insulating supporting member. A solder resist layer would be redundant and wasteful.

Therefore, applicant respectfully submits that at least the step of "removing the carrier tape to uncover the entire first side of the metal layer" and the combination of the removing step and the step of "then applying an insulating layer to the first side uncovering a portion of the first side of the patterned metal layer" are missing from the Fukutomi publication.

The Office Action refers to the layer 53 as anticipates the insulating layer in step (f) of claim 18.[19] However, layer 53 sits on the same side of the metal pattern where the semiconductor chip is attached; whereas in claim 18, the insulating layer in step (f) is on the first side of the metal layer while the chip is on the second side.

Because the Fukutomi publication does not disclose the method in claim 18 as a whole, it does not support a prima facie case of obviousness against claim 18 and applicant respectfully submits that claim 18 stands patentable over the Fukutomi reference.

2. The Fukutomi reference does not disclose the two layers required in claim 19.

Claim 19 properly depends from claim 18 with additional requirement that the insulating layer on the first side of the metal pattern be thinner than the removed insulating carrier tape. Since the Fukutomi reference does not disclose an insulating layer removed from the metal pattern as required in claim 18, it does not disclose the

[18] Id. ¶ [168] lines 9 through 10.
[19] The Office Action, supra, page 3.

method in claim 19 as a whole, and therefore it does not support a prima facie case of obviousness against claim 19. Applicant respectfully submits that claim 19 also stands patentable over the Fukutomi reference.

For the reason presented above, applicant respectfully submits that because the Fukutomi reference does not disclose claim 18 and 19 as a whole, the obviousness rejections against claim 18 and claim 19 are improper. Applicant respectfully requests the Board to reverse the final rejection and allow claim 18 and its dependent claim 19 on appeal.

Respectfully submitted,
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CLAIMS APPENDIX

The claims on appeal read as follows:

18. A method for packaging an integrated circuit chip, comprising:

providing an integrated circuit chip;

providing an insulating carrier tape with a patterned metal layer with a first side adhering to the insulating carrier tape;

positioning the integrated circuit chip over a second side of the metal layer and electrically connecting the integrated circuit chip to the metal pattern;

encapsulating the chip and the electrical connections;

removing the carrier tape to uncover the entire first side of the metal layer; and

then applying an insulating layer to the first side uncovering a portion of the first side of the patterned metal layer.

19. The method of claim 18, in which the insulating layer is thinner than the insulating carrier tape.

EVIDENCE APPENDIX

None

RELATED PROCEEDINGS APPENDIX

None